Amendments to the Specification:

Please replace paragraphs 007, 008, 009, 0010, 0011, 0017, 0018, 0024, 0025, 0031, 0032, 0034, 0035, 0038, 0039, 0040, 0041, 0043, 0044 with the following replacement paragraphs:

007 Common uses of non-volatile memory include portable computers, personal digital assistant (PDA) devices, digital cameras, and cellular telephones. In these devices, both program code and system data, such as configuration parameters and other firmware, are often stored in flash memory because of the compact storage and relative ease of software upgradeability. The use of flash memory, for example, to store upgradeable ~~ungradable~~ data has necessitated the development of mechanisms to protect the data from unintended erasure or reprogramming.

008 Memory arrays for use in non-volatile memory devices can be configured such that their memory cells are generally arranged in rows and columns. Typically, the gates of the transistors within the same row are connected to each other and to a common word line. Similarly, the drain electrodes of the transistors within the same column can be connected to each other and to a common bit line. In addition, the source electrodes of the transistors may be connected to each other via a common source line. To program a selected memory cell in a selected row and a selected column, a programming voltage can be applied to ~~either or~~ both the word line and the bit line which may be connected to the selected memory cell.

009 Memory arrays utilized to form EEPROM, EPROM, or Flash memory cells can use redundant memory elements (i.e., cells and accompanying word lines and bit lines organized as rows [[or]] and columns) to compensate for production errors. Specifically, after the production of a complete memory array, a post-production test in the memory array can be generally performed. This post-

production testing may indicate that a particular column, row or cell of the memory array is defective. A redundant memory element can then be substituted for the defective ~~elements~~ element. This substitution typically occurs after the entire memory array has been manufactured. By allowing a defective memory element to be replaced by a redundant element after production, the memory array can still be used.

0010 Non-volatile memory can be utilized to store information necessary to repair defective rows and/or columns of memory arrays. The portion of the memory array that is utilized to store this repairing information ~~or data~~ can be referred to as the "information array." The repairing information is generally ~~read-out~~ obtained to a volatile latch array after the associated computer system is powered-up. In order to save area or reduce associated circuit complexity, the information array can be placed together with the main array, such that both of these arrays share the same general "periphery circuit" and "bit lines." The repairing information, however, cannot be read-out correctly if the corresponding bit lines are defective. In other words, defective rows or columns cannot be repaired if [[the]] a defective ~~rows or~~ columns itself [[are]] is relied upon to read-out the information array. Thus, the repairing efficiency in such configurations is quite low.

0011 Based on the foregoing, the present inventor has come to the conclusion that a need exists for methods and systems, which would result in a dramatic increase in the repairing efficiency of rows and columns in non-volatile memory arrays. The present inventor, in particular, has concluded that the utilization of an Error Correction Coding (ECC) scheme can assist in improving this repairing efficiency.

0017 The above and other aspects of the present invention are achieved as is now described. Methods and systems for improving repairing efficiency in non-volatile memory are disclosed herein. Row and/or column repairing data may be read from an information array associated with the non-volatile memory. The repairing data is generally read to a volatile latch array associated with the non-volatile memory. An error correction coding circuit (ECC) circuit can be enabled during reading of the repairing data ~~to thereby identify and repair defective row or columns~~ for identifying and repairing defective rows or columns associated with the non-volatile memory, ~~regardless of the corruption of the columns~~ despite and error caused by a defective column. The ECC circuit can thus be enabled during an access of a main array associated with the non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of a defective row or column. This particular address may comprise, for example, a Y-address corresponding to a defective column. When accessing an information row, the ECC function described herein can be unconditionally enabled to ensure that repairing information can be correctly ~~read-out~~ obtained. When accessing the main array, such an ECC function is generally enabled if the Y-address is coincident with a failed Y-address.

0018 A read circuit is generally linked to the main array to thereby permit data to be read from the main array and transmitted to the ECC circuit. The ECC circuit is generally connected to the volatile latch array to thereby permit data to be transferred from the ECC circuit to the volatile latch array. The decoder circuit is generally linked to the volatile latch array and ~~ECC circuit, while the decoder circuit is generally linked~~ to the information array, at least one spare row, and the main array, wherein the main array can include ~~includes~~ a normal array and one or more spare columns. The main array may also be linked to the information array such that the information array is considered part of the main array or a separate array, which shares the same circuit periphery with the main array. The volatile latch

array can be connected to the decoder circuit to thereby permit data contained within the volatile latch array to be accessed by the decoder circuit.

0024 FIG. 5 illustrates a block diagram illustrative of a row and column repair scheme for non-volatile memory; and

0025 FIG. 6 depicts a block diagram illustrative of a row and column repair scheme for non-volatile memory utilizing an error correction coding (ECC) circuit, in accordance with a preferred embodiment of the present invention.

0031 There are a variety of non-volatile memory devices that may be utilized to implement non-volatile memory 14. Thus, as illustrated in FIG. 2, an EPROM 30 may be utilized. An EPROM (Erasable Programmable Read-Only Memory) is generally a type of non-volatile memory chip that can be programmed after it is manufactured. As depicted in FIG. 3, an EEPROM 34 may be ~~relied upon as a~~ used as the non-volatile memory device. An Electrically Erasable and Programmable Read Only Memory ("EEPROM") is a non-volatile memory device that retains its memory even after power is shut down.

0032 Finally, as depicted in FIG. 4, a Flash memory 36 may ~~be another type of non-volatile memory device that can~~ be utilized in accordance with the invention described and claimed herein. Flash memory is similar to EEPROM memory in function; however, it must be erased in blocks, whereas EEPROM can be erased one byte at a time. Because of its block-oriented nature, Flash memory is preferably utilized as a supplement to or replacement for hard disks in portable computers. Flash memory can either be constructed into the unit or available in the form of a PC card that can be plugged into a PCMCIA slot.

0034 FIG. 5 illustrates a block diagram 48 illustrative of a row and column repair scheme for non-volatile memory. Non-volatile memory can be utilized to store information ~~or data~~ regarding correction ~~or repair~~ of array rows and/or columns. A portion of non-volatile memory in which repair information is read out of memory is generally referred to as the "information array." Repairing information or data is thus read out of information array 52 to a volatile latch array 60 after the associated computer system is powered-up (i.e., initiated).

0035 In order to save area or reduce the circuit complexity, information array 52 is generally placed with the main array 50. Main array 50 is composed of a spare row 54 and a section 56 comprising a "normal array" and a spare column. Thus, information array 52 and main array 50 share the same "periphery circuit" and "bit lines." The repairing information, however, cannot be read-out correctly if the corresponding bit lines are defective ~~or corrupted~~. In other words, defective ~~or corrupted~~ columns may not be repaired if the defective ~~or corrupted~~ column is utilized to read-out information array 52.

0038 FIG. 6 depicts a block diagram 49 illustrative of a row and column repair scheme for non-volatile memory utilizing an error correction coding (ECC) circuit, in accordance with a preferred embodiment of the present invention. Note that in FIGS. 5 and 6, analogous or similar parts are indicated by identical reference numerals. The configuration depicted in block diagram 49 thus depicts a redundancy scheme involving the use of Error correction coding (ECC) to improve the efficiency of row and column repairing. Error correction codes are generally utilized to correct certain classes of errors in memory storage devices, such as non-volatile memory devices, to greatly reduce the probability of an error affecting the memory output. ECC is generally an encoding method that permits the detection and correction of errors that can occur during data storage and transmission.

0039 An error correction coding (ECC) circuit 70 is linked to volatile latch array 60, which in turn is connected to decoder circuit 62. ECC circuit 70 can be enabled through ECC enabling circuit 72, which is connected to ECC circuit 70. Read circuit 58 can access main memory 50 and transfer data to ECC circuit 70. To achieve improved row and column repair, information ~~or data~~ may be read from information array 52 to volatile latch array 60 after system power-up. During access of main array 50, ECC circuit 70 is enabled to ~~repair~~ correct correctable errors if a Y-address corresponds to an address indicative of a ~~corrupt or~~ defective row and/or column. During the ~~read-out of~~ obtained of repairing information from information array 52, ECC circuit 70 is always enabled to ~~repair~~ correct any correctable errors of data. The correct repairing information can be read out of information array 52 even if some of the selected columns are defective ~~or corrupted~~ during access of information array 52.

0040 The configuration illustrated in FIG. 6 enables ECC circuit 70 to correct the correctable error when accessing repairing formation from information array 52. The repairing information can be ~~read~~ obtained correctly even if a corrupted bit is ~~defective or corrupted bits are~~ present. This configuration thus improves the repairing efficiency when the information array 52 shares the same read/write circuit and bit lines with main array 50. If an ECC circuit, such as ECC circuit 70, is not available, ~~defective~~ corrupted bits in information array 52 will render the chip unrepairable.

0041 FIG. 6 thus depicts a configuration that may be utilized to improve column and/or row repairing efficiency in non-volatile memory devices, such as, for example, EPROM, EEPROM and Flash memory devices. Column and/or row repairing data may be read from information array 52, which is associated with the non-volatile memory and can form part of main array 50. This repairing data is generally read to ~~a~~ volatile latches ~~latch~~ (e.g., volatile latch array 60) associated with the non-volatile memory. ECC circuit 70 can be enabled during reading of the

repairing data ~~to thereby identify and repair~~ for identifying and repairing defective rows and/or columns associated with the non-volatile memory, ~~regardless of the corruption of the columns~~ despite an error in the repairing information caused by a defective column. ECC circuit 70 can thus be enabled thus be enabled during an access of main array 50 (i.e., which is associated with the non-volatile memory) to thereby correct a correctable error ~~errors~~ if a particular address corresponds to an address of at least one defective row and/or column. This particular address may, for example, comprise a Y-address corresponding to a defective column ~~or row~~.

0043 The number of spare columns ~~depends on the coding of ECC circuit 70 and~~ determines the maximum number of defective columns on a normal array that can be repaired. ~~For example, in a scenario in which~~ In one embodiment, 512 columns are ~~designated in a normal~~ in the array, ~~and a~~ the data bus ~~comprises~~ is 16 bits, ~~assuming that~~ and a (16,11) Hamming code ~~(5,16)~~ is used. A total of 20 spare columns are provided, each spare being assignable to one of four sets of four I/O terminals and five spares being reserved for each such set of four I/O terminals. ~~utilized and additionally assuming that the maximum number of defective columns that can be repaired is 4, then the number of spare columns required can be calculated as 20 based on the value 4x5. This holds true because 5 spare columns are generally required to repair 4 defective columns.~~

0044 ~~Traditionally, one spare column is generally required to repair one defective column for one "specific IO" (i.e., there are 16IO if a data bus is 16 bits). At least one spare column, however, must be placed per IO because the defective column could be located on any one IO. Thus, 16 spare columns are needed to repair one defective column. To improve the repairing efficiency, two IO with increasingly complicated designs could share one spare column. As a result, at least 8 spare columns may be required. Thus, in accordance with the method and system of the present invention, one or more spare columns (i.e., 5 in the aforementioned example) are required to repair one defective column in any IO.~~

~~(Note that Hamming code (5,16) is well known in the art and is described generally~~ Traditionally, each spare column is reserved for repairing one column corresponding to a specific I/O terminal. If there are 16 I/O terminals for a 16-bit data bus, then 16 spare columns would normally be required to support a one-time repair of any possible column out of the 16 columns accessed at one time. To improve repairing efficiency, the columns for two or more I/O terminals can be made to share a single column, in a more complicated design. In the specific embodiment described above, all columns associated with a set of four I/O terminals share a single set of five spare columns. The (16,11) Hamming code is well known in the art and is described at pg. 64 of "Error Control Coding: Fundamentals and Applications," by Shu Lin & Daniel J. Costello, Jr.).